METHOD FOR TIME-DOMAIN SYNCHRONIZATION ACROSS A BIT-SLICE DATA PATH DESIGN

ABSTRACT OF THE DISCLOSURE

A bit slice data path design is provided. Multiple chips are coupled to a data bus and configured to process a slice of data for the data bus. One chip in the design is designated as a master chip and the other chips are designated as slaves. A master chip sends a signal from a first time domain to a second time domain through a synchronization circuit. When the signal has been synchronized to the frequency of the second time domain, the signal is sent to the slave chips through a connection. The signal is also looped back to the second time domain in the master chip so that the signal reaches the second time domain in the master and slave chips in the same clock cycle.